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EXAMINER	
DUONG, THOI V	
ART UNIT	PAPER NUMBER
2871	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/049,792	AOKI, HIRONORI	
	Examiner	Art Unit	
	THOI V. DUONG	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 07, 2009 has been entered.

Accordingly, claims 1, 3 and 22 were amended, and claims 4, 7, 13, 14 and 19-21 were cancelled. Currently, claims 1-3, 5, 6, 8-12, 15-18 and 22 are pending in this application.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 3 and 22 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1, 3 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The phrase "said connecting part is formed as large as possible, as long as said connecting part is not electrically connected to an adjacent pattern" was held to render the claims indefinite since it is not sure how much

large is considered as large as possible to satisfy the limitations of the claims. Moreover, the specification also lacked some standard for measuring the degree intended.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 2, 5, 6, 8-12, 15-18 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Dohjo et al. (Dohjo, US 5,835,177).

Re claim 1, as shown in Figs. 1, 3, 5 and 13, Dohjo discloses an array substrate 100 comprising:

a display area (TFT region) in which pixel electrodes 131 are formed; a scanning line 111 arranged between the pixel electrodes 131;

a signal line 110 crossing over the scanning line 111 interposing an insulating layer 115 therebetween;

a terminal 152 (first terminal) to which a scanning signal is applied;

an extended scanning line 125a formed from a layer of said signal line 110 for electrical connecting the scanning line 111 with the terminal 152; and

a connecting part 131 for connecting said scanning line 111 with said extended scanning line 125a by said pixel electrodes (Fig. 3).

According to Figs. 1 and 3, it is clear that said connecting part 131 is formed with a size as large as possible to maintain the connecting with said scanning line 111 adjacent to said connecting part and said connecting part is not electrically connected to an adjacent pattern such as the signal line 110.

Re claim 2, as shown in Figs. 28 and 31, the array substrate further comprises:

an auxiliary capacitance line 113 arranged in parallel to the scanning line 111 (Fig. 28 and col. 23, lines 54-55);

a collected auxiliary capacitance line (dotted line of storage capacitor-line connecting section 190 in Fig. 28) arranged in parallel to the signal line 110 and electrically connected to the auxiliary capacitance line 113;

a terminal (second terminal) to which a common signal is applied (at top left of Fig. 28); and

an extended auxiliary capacitance line 125 for connecting the collected auxiliary capacitance line with the terminal for the common signal (Fig. 31), said extended auxiliary capacitance line being formed only of the same conductive film as for said signal line (col. 23, lines 54-64).

Re claims 5 and 8, as shown in Fig. 31, Dohjo discloses that the collected auxiliary capacitance line and the extended auxiliary capacitance line are electrically connected via a conductive film 193 of the same layer as that for the pixel electrode, wherein, re claim 9, the extended auxiliary capacitance line 125 is electrically connected to the collected auxiliary capacitance line at the neighborhood of the display area

through a contact hole 192 and electrically connected to the terminal for the common signal through a contact hole 194 at the neighborhood of the terminal;

wherein, re claim 10, the auxiliary capacitance line 113, the collected auxiliary capacitance line and the scanning line 111 are formed from the conductive film of same layer (col. 23, lines 42-45);

wherein, re claim 11, the collected auxiliary capacitance line and the extended scanning line are crossing interposing an insulating layer 117 therebetween (Fig. 31); and

wherein, re claim 18, the extended auxiliary capacitance line 125 is formed in a grid like shape at a region 190 in which the collected auxiliary capacitance line and the extended auxiliary capacitance line are overlapped within a connecting portion between the collected auxiliary capacitance line and the extended auxiliary capacitance line (see Fig. 31).

Re claim 16, Dohjo also discloses in another embodiment that the extended scanning line and the pixel electrodes are formed from the conductive film of same layer (col. 5, lines 27-45). Since the extended auxiliary capacitance line is formed at the same layer as the extended scanning line, the extended auxiliary capacitance line and the pixel electrodes are also formed from the conductive film of same layer.

Re claim 6, Dohjo discloses that the extended scanning line 125a is electrically connected to the scanning line 111 through contact holes 153, 154 at the neighborhood of the display area and electrically connected to the terminal 152 for the scanning signal through contact holes 155, 156 at the neighborhood of the terminal (see Figs. 1 and 3).

Re claim 12, Dohjo discloses that aluminum or aluminum alloy is used for material of the scanning line (col. 7, lines 16-27).

Re claim 15, Dohjo discloses that the scanning line 111 and the extended scanning line 125a are electrically connected via a conductive film of the same layer 131 as that for the pixel electrode.

Re claim 17, Dohjo discloses that the extended scanning line 125a is formed in a grid like shape at a region (Base section in Fig. 3) in which the scanning line and the extended scanning line are overlapped within a connecting portion between the scanning line and the extended scanning line.

Claim 22 is also rejected since it contains the limitation of claims 1 and 2.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-3, 5, 6, 8-12, 15-18 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dohjo et al. (Dohjo, US 5,835,177) in view of Ahn (US 6,288,414 B1).

Re claim 1, as shown in Figs. 1, 3, 5 and 13, Dohjo discloses an array substrate 100 comprising:

a display area (TFT region) in which pixel electrodes 131 are formed; a scanning line 111 arranged between the pixel electrodes 131;

a signal line 110 crossing over the scanning line 111 interposing an insulating layer 115 therebetween;

a terminal 152 (first terminal) to which a scanning signal is applied;

an extended scanning line 125a formed from a layer of said signal line 110 for electrical connecting the scanning line 111 with the terminal 152; and

a connecting part 131 for connecting said scanning line 111 with said extended scanning line 125a by said pixel electrodes (Fig. 3).

Fig. 3 of Dohjo shows that the connecting part is formed with a size to maintain the connecting with said scanning line 111 adjacent to said connecting part such that said connecting part is not electrically connected to an adjacent pattern such as the signal line 110. However, Dohjo does not disclose that said connecting part is formed as large as possible.

As shown in Figs. 3, 5F, 6, 7B, 8A and 8B, Ahn discloses a pad structure comprising a gate pad 115/117 and a gate pad terminal 165 (connecting part) formed in such a manner as to have many small contact holes to enlarge the contact area in order to improve contact resistance between the pad and the pad terminal (Abstract and col. 8, lines 3-24). Accordingly, the connecting part is obviously formed as large as possible by forming many small contact holes so as to obtain a small value contact resistance.

Fig. 3 of Ahn also shows that the connecting part 165 is not electrically connected to an adjacent pattern such as the data line 135 because such connection would result in a short circuit which fails the display.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the array substrate Dohjo with the teaching of Ahn by forming the connecting part as large as possible, as long as said connecting part is not electrically connected to an adjacent pattern, in order to keep contact resistance at a low level and maintain the scan signal in their original state (col. 3, lines 28-30). Accordingly, it is also obvious that a small value contact resistance is obtained to prevent the common signal from delaying.

Re claim 2, as shown in Figs. 28 and 31, the array substrate further comprises:

an auxiliary capacitance line 113 arranged in parallel to the scanning line 111 (Fig. 28 and col. 23, lines 54-55);

a collected auxiliary capacitance line (dotted line of storage capacitor-line connecting section 190 in Fig. 28) arranged in parallel to the signal line 110 and electrically connected to the auxiliary capacitance line 113;

a terminal (second terminal) to which a common signal is applied (at top left of Fig. 28); and

an extended auxiliary capacitance line 125 for connecting the collected auxiliary capacitance line with the terminal for the common signal (Fig. 31), said extended auxiliary capacitance line being formed only of the same conductive film as for said signal line (col. 23, lines 54-64).

Re claims 5 and 8, as shown in Fig. 31, Dohjo discloses that the collected auxiliary capacitance line and the extended auxiliary capacitance line are electrically connected via a conductive film 193 of the same layer as that for the pixel electrode,

wherein, re claim 9, the extended auxiliary capacitance line 125 is electrically connected to the collected auxiliary capacitance line at the neighborhood of the display area through a contact hole 192 and electrically connected to the terminal for the common signal through a contact hole 194 at the neighborhood of the terminal;

wherein, re claim 10, the auxiliary capacitance line 113, the collected auxiliary capacitance line and the scanning line 111 are formed from the conductive film of same layer (col. 23, lines 42-45);

wherein, re claim 11, the collected auxiliary capacitance line and the extended scanning line are crossing interposing an insulating layer 117 therebetween (Fig. 31); and

wherein, re claim 18, the extended auxiliary capacitance line 125 is formed in a grid like shape at a region 190 in which the collected auxiliary capacitance line and the extended auxiliary capacitance line are overlapped within a connecting portion between the collected auxiliary capacitance line and the extended auxiliary capacitance line (see Fig. 31).

Re claim 16, Dohjo also discloses in another embodiment that the extended scanning line and the pixel electrodes are formed from the conductive film of same layer (col. 5, lines 27-45). Since the extended auxiliary capacitance line is formed at the same layer as the extended scanning line, the extended auxiliary capacitance line and the pixel electrodes are also formed from the conductive film of same layer.

Re claim 6, Dohjo discloses that the extended scanning line 125a is electrically connected to the scanning line 111 through contact holes 153, 154 at the neighborhood

of the display area and electrically connected to the terminal 152 for the scanning signal through contact holes 155, 156 at the neighborhood of the terminal (see Figs. 1 and 3).

Re claim 12, Dohjo discloses that aluminum or aluminum alloy is used for material of the scanning line (col. 7, lines 16-27).

Re claim 15, Dohjo discloses that the scanning line 111 and the extended scanning line 125a are electrically connected via a conductive film of the same layer 131 as that for the pixel electrode.

Re claim 17, Dohjo discloses that the extended scanning line 125a is formed in a grid like shape at a region (Base section in Fig. 3) in which the scanning line and the extended scanning line are overlapped within a connecting portion between the scanning line and the extended scanning line.

Re claim 3, as shown in Figs. 28 and 31, Dohjo discloses an array substrate 100 comprising:

a display area (TFT region) in which pixel electrodes 131 are formed; a scanning line 111 arranged between the pixel electrodes 131;

a signal line 110 crossing over the scanning line 111 interposing an insulating layer 115 therebetween;

an auxiliary capacitance line 113 arranged in parallel to the scanning line 111 (Fig. 28 and col. 23, lines 54-55);

a collected auxiliary capacitance line (dotted line of storage capacitor-line connecting section 190 in Fig. 28) arranged in parallel to the signal line 110 and electrically connected to the auxiliary capacitance line 113;

a terminal (second terminal) to which a common signal is applied (at top left of Fig. 28);

an extended auxiliary capacitance line 125 formed from a conductive film for connecting the collected auxiliary capacitance line with the terminal for the common signal (Fig. 31); and

a connecting part 193 for connecting said collected auxiliary capacitance line with said extended auxiliary capacitance line 125 by said pixel electrodes 131,

wherein the extended auxiliary capacitance line 125 is formed from a layer of said signal line 110 (col. 23, lines 54-64).

However, Dohjo does not disclose that said connecting part is formed as large as possible, as long as said connecting part is not electrically connected to an adjacent pattern in order to obtain a small value contact resistance, and to prevent said common signal from delaying.

As shown in Figs. 3, 5F, 6, 7B, 8A and 8B, Ahn discloses a pad structure comprising a gate pad 115/117 and a gate pad terminal 165 (connecting part) formed in such a manner as to have many small contact holes to enlarge the contact area in order to improve contact resistance between the pad and the pad terminal (Abstract and col. 8, lines 3-24). Accordingly, the connecting part is obviously formed as large as possible by forming many small contact holes to obtain a small value contact resistance.

Fig. 3 of Ahn also shows that the connecting part 165 is not electrically connected to an adjacent pattern such as the data line 135 because such connection would result in a short circuit which fails the display.

Accordingly, it is also obvious that the teaching of Ahn is applicable to the connecting part for connecting said collected auxiliary capacitance line with said extended auxiliary capacitance line.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the array substrate Dohjo with the teaching of Ahn by forming the connecting part as large as possible, as long as said connecting part is not electrically connected to an adjacent pattern, in order to keep contact resistance at a low level and maintain the scan signal in their original state (col. 3, lines 28-30). Accordingly, it is also obvious that a small value contact resistance is obtained to prevent the common signal from delaying.

Finally, claim 22 is rejected since it contains the limitations of claims 1 and 2.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (571) 272-2292. The examiner can normally be reached on Monday-Friday from 8:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms, can be reached at (571) 272-1787.

/Thoi V. Duong/ - Primary Examiner

July 19, 2009